Title: An embedded implementation based on adaptive filter bank for brain-computer interface systems

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Highlights

- A high accuracy embedded brain computer interface based on motor imagery is proposed.
- EEG signals are filtered dynamically using WOLA methods.
- Both Spatial and spectral features of EEG signals are extracted and classified using CSP and LDA methods respectively.
- The proposed method is implemented on Stratix-IV FPGA.
- HW/SW co-design is applied in order to satisfy the golden triangle: cost, time, and performance.

An embedded implementation based on adaptive filter bank for brain-computer interface systems

Abstract

Background: Brain-computer interface (BCI) is a new communication pathway for users with neurological deficiencies. The implementation of a BCI system requires complex electroencephalography (EEG) signal processing including filtering, feature extraction and classification algorithms. Most of current BCI systems are implemented on personal computers. Therefore, there is a great interest in implementing BCI on embedded platforms to meet system specifications in terms of time response, cost effectiveness, power consumption, and accuracy.

New-Method: This article presents an embedded-BCI (EBCI) system based on a Stratix-IV field programmable gate array. The proposed system relays on the weighted overlap-add (WOLA) algorithm to perform dynamic filtering of EEG-signals by analyzing the event-related desynchronization/synchronization (ERD/ERS). The EEG-signals are classified, using the linear discriminant analysis algorithm, based on their spatial features.

Results: The proposed system performs fast classification within a time delay of 0.430 s/trial, achieving an average accuracy of 76.80% according to an offline approach and 80.25% using our own recording. The estimated power consumption of the prototype is approximately 0.7W.

Comparison-with-Existing-Method: Results show that the proposed EBCI system reduces the overall classification error rate for the three datasets of the BCI-competition by 5% compared to other similar implementations. Moreover, experiment shows that the proposed system maintains a high accuracy rate with a short processing time, a low power consumption, and a low cost.

Conclusions: Performing dynamic filtering of EEG-signals using WOLA increases the recognition rate of ERD/ERS patterns of motor imagery brain activity. This approach allows to develop a complete prototype of a EBCI system that achieves excellent accuracy rates.

Keywords: Embedded brain-computer interface (EBCI), Electroencephalography (EEG), Motor imagery, EEG filter optimization, Weighted overlap-add (WOLA), System on programmable chip (SOPC), Embedded Real-time BCI.

1. Introduction

Improving the quality of life of persons suffering from cerebrovascular accident, spinal cord injury, and other similar illnesses is one of the most challenging tasks facing brain-computer interface (BCI) technologies. These technologies operate in a noninvasive mode [1], which is based on directly capturing electroencephalography (EEG) signals from the scalp using Ag/AgCl electrodes, without the need for any surgical operation. An EEG-based control system can be implemented on the basis of different sensorimotor rhythms (SMRs) such as: event-related desynchronization/synchronization (ERD/ERS) [2], event-related potential (ERP) [3], and P300 speller [4]. Based on these techniques, many applications can be developed to control home equipment [5], bed nursing, multimedia devices [6], games [7], driver assistance systems [8], etc.

The general structure of a BCI chain is presented in Fig. 1. A BCI system is connected to an electronic device, such as a laptop, field-programmable gate array (FPGA), or digital signal processor (DSP), which executes signal processing algorithms that are able to recognize patterns associated with specific brain activity and associate each acquired trial to its corresponding task. This approach is known as the online approach. The other alternative is the offline approach, in which the acquired EEG signal is processed after the recording of many trials [9]. Once the EEG signal is acquired, a machine learning approach is applied comprising three progressive processing stages: EEG filtering, feature extraction, and classification, which are highly application-dependent. Often, these techniques are selected based on the obtained system performance during the discrimination of the mental task in the offline approach. In fact, the system performance represents the ratio of the correctly classified trials to the total processed trials. In this study, these trials are captured as the subject thinks about moving the left or right hand.

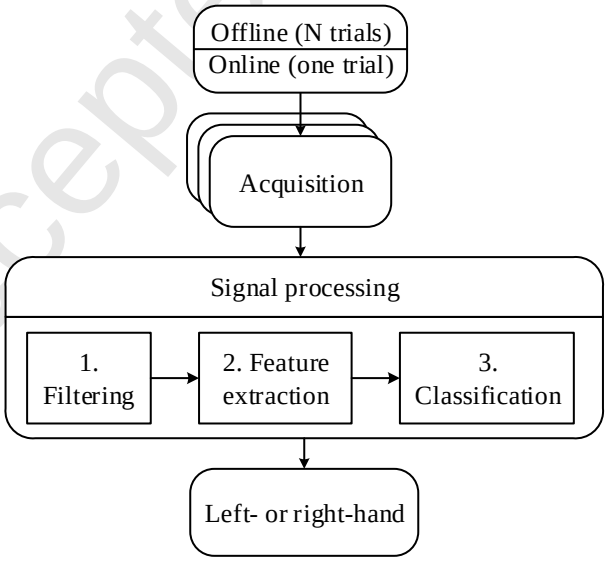

Fig. 1: General structure of BCI chain [10]

During an imagery task, two phenomena appear in the cortical α and β rhythms [11]. Such variations are referred

to as ERD/ERS. For example, when the left-hand movement is performed, the α and β rhythms exhibit a power decrease prior to the actual movement. The ERD/ERS phenomena are quantified as a function of time and space, which is presented as a map to show the frequency oscillation in the brain area. The quantification of the ERD/ERS is highly dependent on the triggers referencing the beginning of each trial. The length before and after the event-related trials are depicted in Fig. 2. The main question of the quantification is how to detect the subject-specific frequencies, which appear during left- and right-hand movements [12]. EEG signal analysis does not imply simple quantification, but also involves elements of pattern recognition. These elements are based on the feature extraction and classification of each event related to their corresponding tasks.

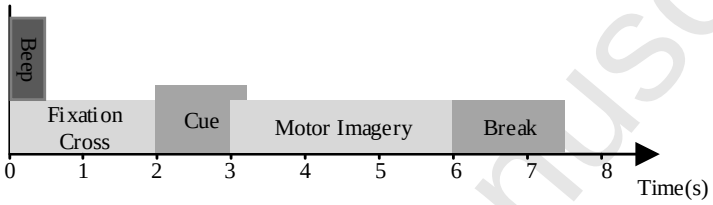

Fig. 2: Timing scheme of the acquisition paradigm

For quantification, one way to define the EEG frequency bands is to identify the frequency band showing statistically significant difference and a solution to compute the spectrum of the EEG signals. The returned bands that show a significant decrease are selected for ERD calculation (α rhythm [8 12] Hz), whereas the bands with a significant power increase are selected for ERS (β rhythm [12 30] Hz). Theoretically, the frequency band cannot be defined for both subjects, owing to the intrinsic variability between subjects [13]. An automatic process can be used to set the frequencies of each subject during the training phase. Other method of frequency band selection is presented in [14]. In fact, the EEG data are analyzed using ERD/ERS pattern as a measure of the degree of event-related changes in power in the theta and alpha bands (lower alpha and upper alpha). The alpha band is determined using the alpha peak during the rest period, as the cut-off hyper-plane, to separate the lower from the upper alpha band. Hence, care has to be taken to ensure that the returned frequency bands represent the cerebral activities that appeared during the event-related trials.

The statistical properties of EEG signals depend on both space and time. For the temporal characteristic, the EEG signals are ever-changing and they can be divided into small epochs in which they are less statistically constant. The epoch can be defined over short-time intervals that can be more representative of the subject's state [9]. Additionally, Saltzberg showed that interval analyses are very useful for evaluating EEG signals [15]. It is important to note that the interval time should be short enough to avoid stationarity problems. The main advantage of the interval analysis is its simplicity of computation, which makes this method attractive for the online quantification of long EEG records. Other advantages are that successive EEG signals are analyzed and stored in real time and the computation time of the specific-subject frequency detection is minimized.

A frequency that contains the only significant changes in ERD/ERS power in narrow and/or fair frequency bands requires a feasible architecture to auto-select the active frequency spectrum of each person. In literature, most time-frequency analysis methods use a fixed time window that starts 0.5 s before the cue, and fixed bands, which are α and β bands [16]. Two major problems are occurred when using the fixed time window and fixed frequency bands. First, using a time window starting 0.5 s before the cue is not always correct, because this assumes that the user will start thinking of a motor imagery task directly after the appearance of the cue without and delay [17]. Second, the motor imagery tasks are different from one subject to another [18]. Furthermore, identifying the subject-specific discriminating frequency components to distinguish between the right- and left-hand patterns is important to establish a sophisticated EBCI system. To address these matters, a dynamic EEG filter based on the WOLA algorithm is proposed.

Unfortunately, the implementation of an EBCI algorithm requires a high-speed computer to process EEG trials, which limits theirs use and portability. This shortcoming is overcome on the basis of reconfigurable architectures such as FPGAs, which offer very high computing performance to satisfy real-time constraints, are less expensive, and exhibit reasonable power consumption. Another reason to use FPGAs for implementing an EBCI system is the possibility to export the critical parts as coprocessors, with the instructions coded in hardware description language (HDL) to be executed in parallel at low clock rates.

Like [19], the current work proposes an embedded implementation of a BCI system based on motor imagery tasks too. However, unlike [19], the current work proposes a new dynamic filtering method which has a low complexity compared to static filtering method. Furthermore, the epochs of the EEG trials are selected dynamically for each user by selecting the timing window containing the most active ERS/ERS patterns. The training phase of the system based on dynamic filtering method becomes too fast, a significant improvement in the occupation of the FPGA and power consumption are achieved. Unlike [19], the presented system is validated according to the offline and online approach.

The remainder of this paper is organized as follows. In Section 2, the related work is presented, as well as hardware-based BCI platforms; Section 3 describes the proposed approach for the EBCI system. In Section 4, the dynamic filter based on the WOLA method is presented and Section 5 presents the specifications of the EBCI system and the embedded implementation of the preprocessing algorithm of motor imagery tasks. Section 6 describes the two validation purposes of the EBCI system, including the offline and online approaches. In Section 7, the obtained hardware and software results are reported. Finally, Section 8 discuss the obtained results and Section 9 concludes the paper and outlines our future work.

2. Related work

. Even if BCI users provide only slight left-right differences accompanied with artifacts, the application of advanced pre-processing techniques can enhance these differences and improve the BCI control accuracy via filtering. Many signal processing techniques have been widely used for pre-processing, based on:

- Using time and frequency domain transforms such as: fast Fourier transform (FFT) and discreet wavelet transform (DWT). For example, FFT can be applied to each channel to perform the discrete Fourier transform computation to efficiently extract the amplitude and the phase of the ongoing EEG signal. The Fourier components located in the μ and β rhythms are selected for pre-processing and then the signal is reconstructed by taking the inverse Fourier transform (IFFT). It is quite obvious that the Fourier transform components are well localized in frequency but not in time. Wavelet coefficients provide a trade-off in time-frequency localization. This technique is successfully used for removing the undesirable signals as long as the signal-to-noise ratio remains high (above *10 dB*). The wavelet technique does not provide good de-noising of EEG signals buried in high-energy noise [20].

- Subtracting artifacts from the acquired signal: This technique requires average artifact template estimation to be subtracted from the original EEG signal. For instance, the average artifact subtraction techniques (AAS) require a high sampling frequency and are just capable of eliminating repetitive artifact patterns [21]. Independent component analysis (ICA) can also be applied to a multichannel EEG signal by decomposing the original one into multiple source components. Some of them, which are related to the ocular activity can be discarded to remove the main ocular artifacts. Unfortunately, some non-ocular data can also be removed and the classification accuracy remains limited [22].

- Using the same static filtering for all subjects, such as finite impulse response (FIR) and infinite impulse response (IIR) filters: FIR filters such as Equiripple and Kaiserwin are based on the Parks-McClellan algorithm using the Remez exchange algorithm and Chebyshev approximation theory to design filters with an optimal fit between the desired and the actual frequency responses [23]. The main classical IIR filters are Butterworth, Chebyshev types I and II, and elliptic, each of which is optimal for a specific context. For example, Butterworth, based on the Taylor series approximation, provides the best representation of an ideal band-pass filter response, in which elliptic filters allow obtaining equal ripples in both the pass-band and stop-band filter limits. The Chebyshev technique minimizes the absolute difference between the ideal and the actual frequency responses over the entire pass-band by incorporating an equal ripple in the pass-band for the type I filter, and an equal ripple in the stop-band for type II. The abovementioned filters are frequently used with an order less than or equal to eight, providing a steep transition band and uniform ripples in the pass-band and stop-band regions. Consequently, the attenuation of the EEG signal in the stop-band region is limited to 6 dB and cannot be pushed to a greater value such as 80 dB [23].

- Using adaptive filtering techniques: the removal of electrooculography (EOG) artifacts from EEG signals presented in [24] applies ICA to extract information from electrodes close to the eyes. Then the interference of EOG with EEG is estimated using the recursive least squares (RLS) algorithm based on the adaptive adjustment of all filters for each ICA by modifying the offset of the total band from 8 to 30 Hz to get higher accuracy.

Similar adaptive filtering techniques are used in [25], where the best band is fixed by optimizing the objective function of the common spatial pattern (CSP). This technique depends on the CSP outputs and can lead to failure when the CSP does not succeed in providing the feature vector and the filtering approach becomes useless. The so-called adaptive signal enhancer (ASE) is defined as an adaptive filter capable of adjusting its parameters in order to minimize the mean square error (MSE). This method is used to detect a single-sweep ERP in the EEG record [26]. Adaptive recursive band-pass filter (ARBF) is employed to estimate and track the center frequency of the dominant signal of each EEG channel. The main disadvantage of the ARBF is that it only updates one coefficient in order to adjust the center frequency of the band-pass filter to match the noise signal provided as an input. Thus, this technique is not suitable for unpredictable noise [27].

Table 1 summarizes a comparison of the advantages and disadvantages of the existing techniques in the literature. In the table, + indicates that the technique is strong in terms of the respective quality, ± is neutral, − represents weakness. For example, in 3EGBCI, the specific-subject frequency bands are extracted adaptively, a fixed time window is used, and the EEG preprocessing is time consuming because the computation load of the algorithms is very high. Even if these techniques are suitable for some subjects and for a specific dataset, they cannot provide the same accuracy for other subjects belonging to other datasets [25]. To address this issue, an adaptive filter is proposed to localize the frequencies that contain the useful information for each subject separately. During the training phase, the proposed system analysis keeps the EEG signal that contains the ERD/ERS effects and applies the CSP and the LDA using a five-fold cross-validation purpose [28]. The predicted classes of the classifier are compared to the correct class to compute the system performance by incrementing by one when the predicted labels matched the target symbols. Finally, each subject has its own frequency components that guarantee the maximum accuracy.

techniques		Adaptivity	Localization of frequency	Timing window	Effectiveness	Computation load
Time & frequency	FFT	-	-	-	-	±
	DWT	-	-	-	±	±
	WOLA	+	+	+	+	±
Subtracting artifacts	AAS	-	-	-	±	+
	ICA	+	±	-	+	-
static filtering	FIR & IIR	-	±	-	±	±
Subtracting artifacts	RLS	+	±	-	±	-
	ASE	+	±	-	±	-
	ARBF	+	+	-	+	-

Table 1: Comparison between the existing techniques

The theoretical aspects of BCI systems have been well developed, and few attempts to implement a complete hardware system have been reported in the literature. In [29], Lin et al., proposed a real-time wireless embedded EEG-based BCI system that includes physiological signal acquisition, wireless transmission, and a dual-core em-

bedded system with multitask scheduling. This system was implemented for real-time driver drowsiness detection and warning. A session of EEG recording is used during the offline approach to train the system by constructing the drowsiness estimation model including the PCA method. The presented system was validated using the online approach and the average system accuracy for five subjects was 74.6%. Aravien et al. [30] developed an embedded system that can be used for controlling electrical devices through EEG signals related to left- and right-hand movements. The system is implemented on FPGA Spartan 6, and the report did not mention any details regarding the processing time, power consumption, or the validation process. In [31], Palumbo et al., designed and implemented an embedded system for EEG acquisition and real-time EEG signal processing, including ICA, Laplacian filter, and FFT. The EBCI system is implemented on a compactRIO, based on an MPC5200 processor that deterministically executes LabVIEW Real-time applications on the reliable Wind River VxWorks real-time operating system. Despite the embedded implementation of the EEG signal processing algorithm, the presented system exhibits high energy consumption, exceeding 8 W. An EBCI-based smart multimedia controller to select music according to the user's EEG feature is proposed in [32]. The system is developed by Microsoft C♯ and implemented on mobile tablet based on an ARM processor. The power consumption of this EBCI system is approximately 127 Mw, despite the use of very simple EEG signal processing algorithms. A FPGA-based steady-state visually evoked potential (SSVEP) BCI multimedia control system is presented in [33], where the system consumes 7 W to process one trial captured through three EEG channels. A hybrid BCI system for a cyber-physical system (CPS) application is proposed in [34]. It consists of a combination of mental-task-based BCI, SSVEP-based BCI, and eyes-closed detection using a two-channels wireless EEG. The embedded CPS system requires 2-4 s to process one trial acquired through three EEG channels and consumes more than 3 W. Lun-DeLiao et al. [8] developed a wearable mobile EEG-based BCI system (WMEBCIS) for long-term EEG required for drowsiness detection. Kuo-kaiShyu [6] implemented a low-cost FPGA-based architecture using the SSVEP to develop a BCI multimedia control system. The same architecture is applied to control a hospital nursing bed. Gao et al. [5] used SSVEP signal to control environmental devices, such as TV and air-conditioners. It is worth noting that the SSVEP systems need gaze movements. Therefore, significant effort is required from the user to acquire EEG signals for such applications. Thus, the SSVEP approach seems to be inappropriate for people with concentration difficulties or with sight problems when the acquisition process becomes unfeasible. Moreover, the SSVEP approach needs fast actions from a user who is directly in front of the stimulation panel [35]. Furthermore, our proposed approach can be adapted to control such applications allowing the user to move freely and interact easily without any constraints. Table 2 summarizes the EBCI systems existing in the literature.

The proposed method combines smoothing time windows and automatic band selection to produce useful EEG information in multichannel recording, and then enhances the system performance. One of the critical issues in ERD/ERS analysis methods is a time required for the localization of frequency bands. Such localization is very difficult, because it requires very significant calculation resources and the parallel treatment of many EEG signal time windows. Thus, the appropriate embedded platform suitable for such application is the FPGA. The WOLA algorithm, frequency selector, feature extraction technique, and the classifier are combined in a single system on a programmable

EBCI system	Channels	Signal processing unit	Analysis procedure	Time per trial (second)	Power consumption (mw)	Validation purposes
Cyber physical system [34]	2	MCF5213, Nordic micro-controller Atmega128	Band-pass filter Fast Fourier Trasnform (FFT) Artificial Neural Network (ANN)	2 to 4	3300	On-line
EBCI [36]	1	Jetson TK (GPU)	Band-pass filter Batch self-organizing maps (bSOM) SVM	7.73	8400	On-line
Movement prediction [37]	32	Xilinx Zynq	Band-pass filter, decimation Variance filter, adaptive threshold, normalization Passive-aggressive	0.64	4120	On-line
Driver drowsiness detection [38]	2	STM32F103CB	Band-pass filter Relative α band power movement power (MP) SVM	2.23	9360	On-line
Low-cost BCI Platform [39]	8	Arduino due MCU	Band-pass filter, ICA AIDA, PCA LDA	2.23	4000	On-line
Home devices [19]	22	Altera Stratix iV	Adaptive filter CSP Mahalanobis distance	0.399	1.067	Off-line
Prosthetic controller [40]	22	Odroid-xu4	Band-pass filter, ICA CSP, PCA, DWT, STFT LDA, KNN, SVM	≥ 0.5	20000	Off-line
Electrical devices Controller [30]	–	FPGA Spartan 6	FIR filter Discrete Wavelet Transform (DWT) SVM	–	–	Off-line
Smart multimedia [32]	3	Mobile tablet, MSP430	Band-pass filter, moving average Fast Fourier Trasnform (FFT) Threshold	–	127	On-line
Command of wheelchair [41]	8	CompactDAQ	Band-pass filter, spatial filter Discrete Wavelet Transform (DWT) ANN	5	2100	On-line
EBCI [31]	3	CompactRIO	ICA, CAR Fast Fourier Trasnform (FFT) Threshold	–	8100	Off-line
Drowsiness detection [29]	4	Training: PC & Test: DSP Dual core	Resampling, Hanning window, FFT, Normalization and moving average PCA Linear regression model	0.1	529.8	On-line and off-line

Table 2: Summarizes of existing EBCI systems

chip (SOPC) based on the Stratix IV development kit.

3. Proposed approach

Figure3 depicts the general structure of the proposed EBCI system. According to the offline approach, trials are extracted from the recording from 0.5 s before the cue. The EEG signals in each electrode are filtered by the WOLA technique. This method allows to keep the useful information in the α and β bands and the narrow band to make sure that the detected tasks are not due to any muscular activity or other limbs [42]. During this step, it is essential to avoid introducing spurious information that can be generated by an inappropriate application of filter parameters that can be conducted to take a false decision [13]. Once the EEG signal in each channel ($Ch_i; i = 1 : N$) is filtered, a feature extraction algorithm is performed to keep the discriminating information between left- and right-hand movements and reduce the size of the EEG signals. One of the widely used algorithms to extract ERD/ERS information is the CSP method [43]. In fact, CSP tries to extract features that are able to maximize the variance of particular tasks and minimize the variance for others [1].

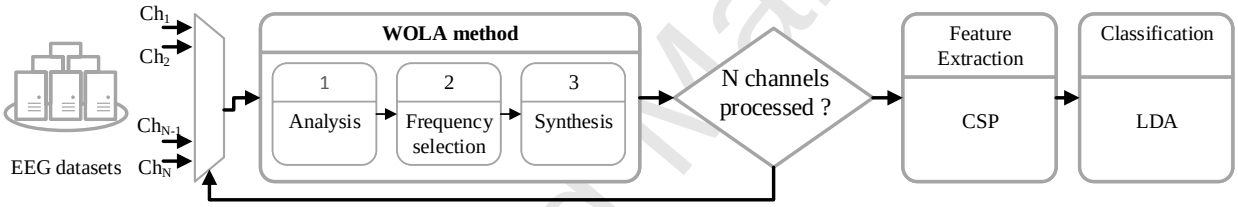

Fig. 3: System block diagram of EEG chain based on dynamic filter

The number of extracted features is too low compared to the input EEG signal, which allows offloading the work of the classifier. More details of the theoretical aspect of CSP are presented in [44]. Finally, the extracted features are classified by a linear classifier such as the linear discriminant analysis (LDA) owing to its low computational cost compared to others, such as the support vector machine (SVM) and K-nearest-neighbor. In fact, the LDA separates the studied tasks by a hyper-plane according to the following equation (Eq. 1):

$$L = W^T E + b \tag{1}$$

where W and b are the hyper-plane coefficients computed and fixed during the training phase. Depending on the sign of L, the classifier will sort each feature E.

3.1. WOLA algorithm

The preprocessing block, which tries to remove artifacts and useless information from EEG recordings, is crucial to maximize the classification accuracy. In the proposed method, a dynamic filter based on the WOLA method is used. In fact, WOLA is highly efficient method used to implement a uniformly distributed multichannel filter bank,

such as the over-sampled generalized DFT filter bank that is usually implemented using an FFT [45]. This method offers a low computational cost, low delay, and a perfect signal reconstruction after keeping the spectrum that seems to contain the useful EEG information. The WOLA algorithm can be divided into three blocks, which are the analysis block, specific-subject frequency selection block, and synthesis block.

3.2. WOLA parameters

In order to implement WOLA filter, there are major parameters that should be well defined. These parameters are:

- N: number of bins.
- R: decimation factor.
- OS: oversampling factor.
- h(n): analysis filter coefficients of length La.
- f(n): synthesis filter coefficients of length Ls = La/R.

The choice and influence of these parameters are the key points in the filter bank design, having consequences on the amount of aliasing, the group delay, the calculation load and, of course, the frequency band resolution. The EEG signal in each electrode is split into N uniform frequency channels arranged from 0 and Fs, where Fs represents the sampling frequency of the EEG signal. In our case, N is set to $\frac{Fs}{2}$ to decompose the input signal into $\frac{Fs}{2}$ channels (x_k) spaced with a step of 1 Hz. The second parameter is the decimation factor R, which is used to correctly interpret aliasing behavior in the filter bank. In fact, the decimation of the EEG signal by a factor R factor corresponds to a compression in the time domain, which corresponds to an expansion in frequency domain. However, the inverse, called interpolation, corresponds to an expansion in time domain and a compression in the frequency domain. Understating decimation and interpolation is very important in order to choose the appropriate WOLA parameters. To avoid the aliasing after the decimation and satisfy the Nyquist criteria, the bandwidth of EEG signal should not be larger than $\frac{Fs}{2R}$. Increasing the decimation factor R, while keeping the same number of channels N, moves the interpolated EEG spectra closer to each other. Usually, an additional parameter is defined to represent the closeness of the interpolation spectra of EEG signals. This parameter is called the oversampling factor ($OS = \frac{N}{R}$). An increase in the OS parameters automatically causes an increase in the calculation load. The last parameters are the analysis filter coefficient ($h(n)$) and synthesis filter coefficient ($f(n)$), which allow, respectively, isolating channel (x_k) and removing images.

3.3. Analysis and synthesis block of WOLA algorithm

The first section of the WOLA filter is the analysis block depicted in Fig. 4. The input EEG signal is divided into different blocks of length R. Each block is weighted by the filter coefficients h(n) computed according to the FIR filter, because its impulse response had a finite duration as required in the time-folding operation. For example, Fig. 5 represents an illustration of the WOLA filter response h(n) in our case, where each frequency channel is centered on

frequency $k = 0$ to $\frac{Fs}{2} - 1$, with a bandwidth equal to 1 Hz. After applying low-pass filter, the EEG signal is divided into many blocks (*Bi*) of length *La* to be overlap-added together, giving a time segment of length *La*. Subsequently, the FFT is applied on the resulted signal to compute the power spectrum density (PSD) in each frequency channel. Once the spectrum is computed, each spectrum is multiplied by a complex exponential $e^{-\frac{j2\pi NmR}{La}}$ in order to shift the spectrum to the origin of the axis.

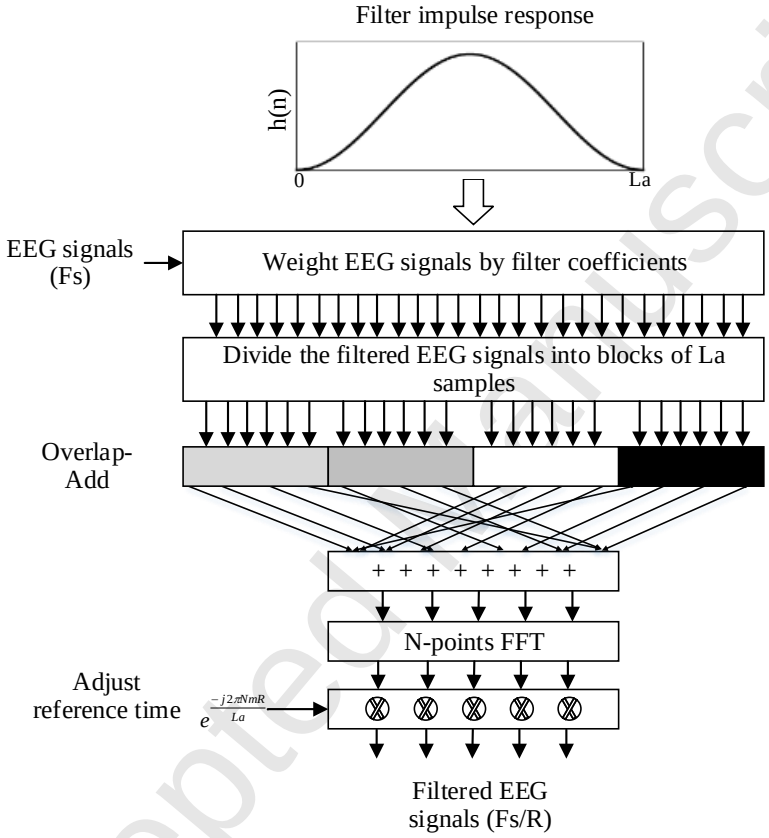

Fig. 4: Analysis block of WOLA algorithm

The third step of the WOLA method is the synthesis block, which corresponds to the reciprocal of the analysis process. The synthesis block interpolates all channel signals back to their high sampling rate by the factor *R*, and modulates them back to their original spectral location by multiplying all selected spectra by $e^{\frac{j2\pi NmR}{La}}$. Instead of using FFT, the synthesis block is applies the IFFT to transform the spectrum back to the time domain. The reconstructed signals should contain just the EEG rhythm selected by the specific-subject frequency selection block, which is the focus of the following section.

3.4. Specific-subject frequency selection

The second block of the WOLA technique is the specific-subject frequency selection (SSFS) algorithm, the purpose of which is to identify and detect the useful EEG spectrum computed by the analysis block. Based on statistical

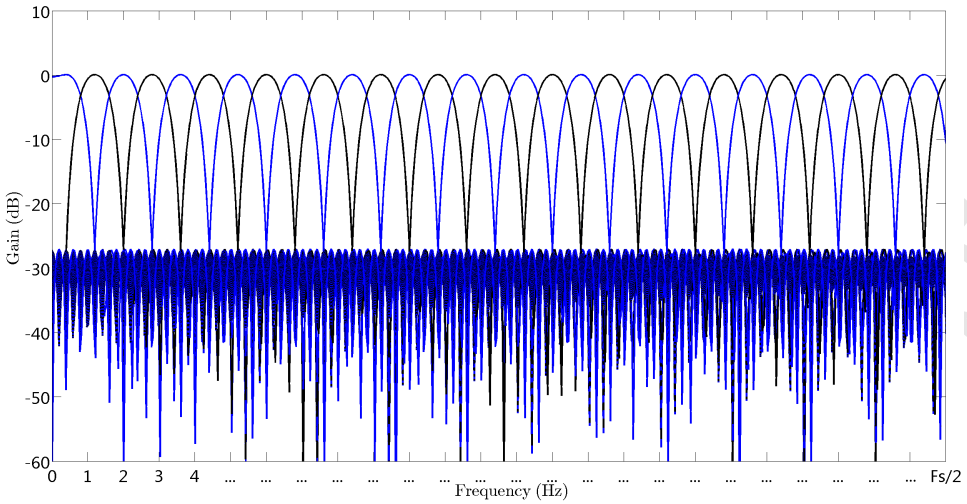

Fig. 5: WOLA filter response

analysis, this block adjusts its parameters to detect the spectrum that seems to contain the information related to left- or right-hand movements. This approach resolves the problem of the static EEG filtering, which delimits the bandwidth of the filter from the beginning without considering the frequency inter-variability between subjects [13]. In the proposed method, three techniques, i.e., hypothesis test (HT), smoothed nonlinear energy operator (SNEO), and ERD/ERS analysis (ERDSA), are used for this purpose.

3.4.1. Hypothesis test (HT)

This method expresses the presence or the absence of the useful information into two hypotheses ($H0$ and $H1$).

$$\begin{cases} \text{Hypothesis 0 } (H_0)\text{: EEG signal contains artefacts } S_K = N_K \\ \text{Hypothesis 1 } (H_1)\text{: EEG signal free of artifacts } S_K = I_K. \end{cases}$$

where S_k, N_K, and I_k represent the EEG signals and the noise at channels K. $H0$ and $H1$ are the two hypotheses between which the SSFS block needs to makes a decision. In fact, the SFFS block make a decision about the presence or absence of the useful information according to this rule:

$$\begin{gathered} H_0 \\ y \underset{<}{\overset{>}{=}} \theta \\ H_1 \end{gathered}$$

where y is the test statistic and θ is threshold considered to decide between the presence or the absence of useful information in EEG signals. The performance of the energy detection can be measured by the probability of false alarm (P_{FA}) and the probability of detection (P_D). P_{FA} and P_D are two statistical measurements defined by:

$$P_{FA} = p(y > \theta; H_0) \tag{2}$$

$$P_D = p(y < \theta; H_1) \tag{3}$$

It is well known that EEG signals have a Gaussian distribution. For this reason, the threshold θ is computed according to the following equation [9, 46]:

$$\theta_D = \sigma_w^2(Q^{-1}(P_F A)\sqrt{2N} + N) \tag{4}$$

where Q^{-1} is the inverse of Gaussian Q-function, σ_w is the variance of noise, N is the number of samples, and P_{FA} is fixed to 0.01.

3.4.2. Smoothed Nonlinear Energy Operator (SNEO)

The smoothed nonlinear energy operator (SNEO) was used to emphasize the artifacts that corrupt the useful information of EEG signals [47].SNEO is an efficient method for detecting spike-like signals, owing to its sensitivity to instantaneous changes in energy. The nonlinear energy operator ϕ is defined as follows:

$$\phi[x(n))] = x(n)^2 - x(n+1) * x(n-1) * \omega(n)) \tag{5}$$

where $*$ is the convolution operator and $\omega(n)$ is a smoothing window function. The SNEO threshold is defined as follows:

$$T = \zeta \frac{1}{N} \sum_{i=1}^{N} \omega(x(n)) \tag{6}$$

where ζ is the scaling factor. It is determined based on the experiments during the training phase of the BCI system. The estimated value of ζ is approximately 5^{-3}, which allows maximizing the system accuracy for all subjects.

3.4.3. ERD/ERS analysis (ERDSA) algorithm

The proposed method consists of selecting the EEG reactivity based on the analysis of the ERD and ERS phenomena. Figure 6 shows the different parts of this method. In fact, the analysis process starts by computing the ERD/ERS, which are defined respectively as the percentage of power decrease or increase, according to the following expression:

$$ERD/ERS\,(f,n) = \frac{P(f,n) - P_{ref}(f)}{P_{ref}(f)} \tag{7}$$

where $P(f,n)$ represents the PSD in each point and P_{ref} describes the spectrum average of reference signals recorded before before left- or right-hand movements. To determine subject-specific frequency bands, the ERD/ERS block detects the ERD peaks, which have a value less than $\frac{3}{2}min(P_{ref}$. While the returned ERS spectra are the peaks which are more than $\frac{2}{3}max(P_{ref}$. The frequency point that satisfies these two conditions above should contain a cerebral activity related to left- and right-hand movement, even if the frequency points are not consecutive. Thereafter, the power spectrum computed with the analysis block corresponding to the selected frequencies are keeping while others are set to zero. Finally, the synthesis block reconstructs the EEG signal with only the returned frequencies. Figure 7 depicts an example of a temporal trial taken from channel C3 and C4 for one subject. C3 and C4 channels are selected

because they are characterized by the appearance of rhythmic activity of the motor imagery movement [48]. The first column of the figure represents the EEG signal at channel C3 before and after applying the WOLA method based on ERS/ERS analysis. The second column shows the EEG signal at channel C4 also before and after the application of WOLA.

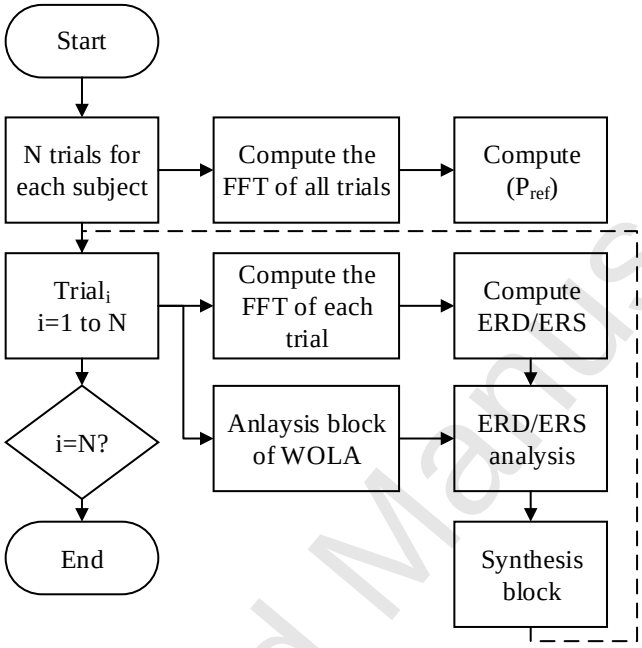

Fig. 6: Specific-subject frequency selection based on ERD/ERS analysis

To show the effectiveness of the proposed method, we propose evaluating the system performance based on its accuracy, which is represented by the ratio of the number of correctly predicted trials to the total number of trials. Another alternative is used to evaluate the proposed approach, consisting of presenting the topography maps at the output of the CSP algorithm. Figure 8 shows the topography of the extracted feature of two trials after applied WOLA filter. The top three topographic represent the ERD/ERS phenomena related to the intention of moving the left hand. For the others, they are visibly associated with the movement of the right hand, because the concentrations of the energy density are localized in the right hemisphere of the brain. These topographic maps show that the WOLA filter has improved the interpretation of these representations compared to other filters applied to the same data bases [44, 49, 50]. Additionally, with the application of the WOLA filter, the topographic maps become more relevant from a neuro-physiological point of view, where the cerebral activities are well shown in the sensory motor area of the brain.

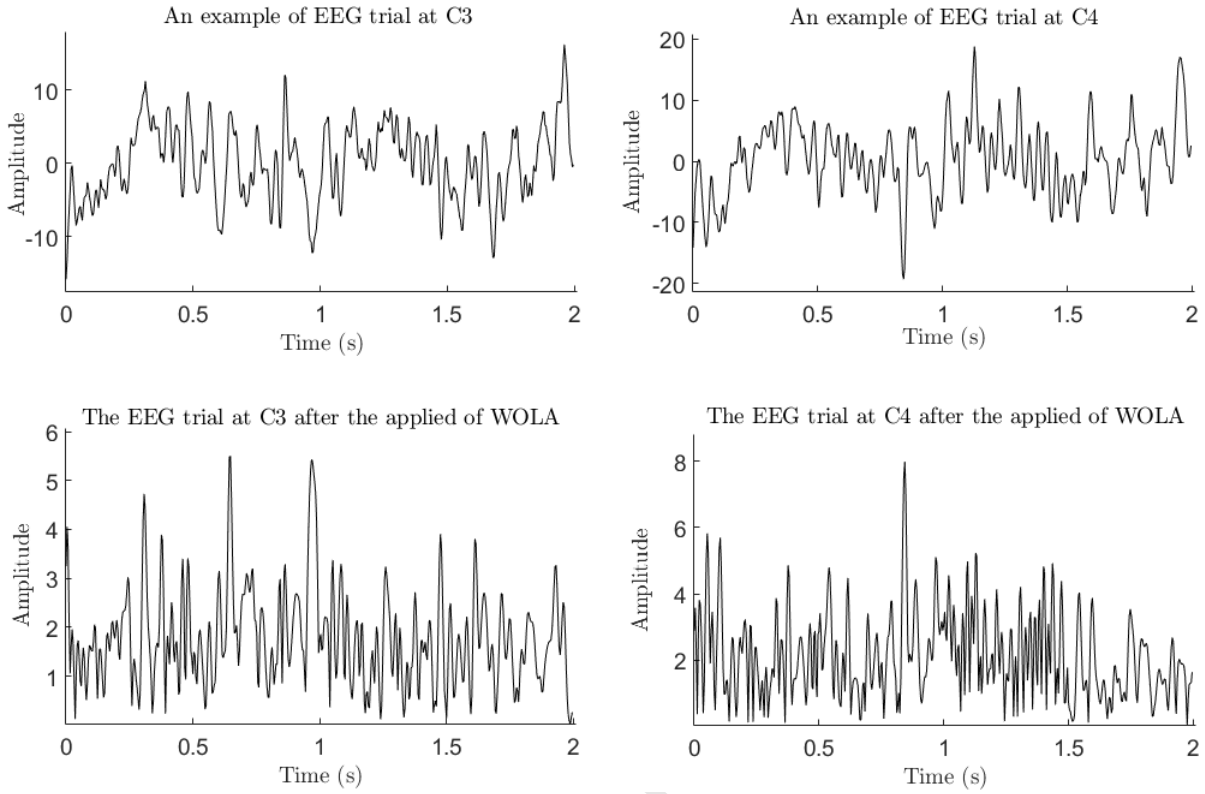

Fig. 7: Example of one trial before and after applied WOLA method based on ERD/ERS analysis

4. Proposed embedded BCI system

4.1. Embedded brain computer interface (EBCI) system specification

Before initiating the implementation of the EBCI system, some system specifications should be taken into consideration, which can be summarized into the following challenges:

1. **High classification accuracy:** the classification of motor imagery tasks should be done with high accuracy (including sensitivity and specificity metrics) and the proposed embedded system has to be sufficiently accurate for a wide range of subjects or patients, with classification accuracy greater than 80%. This rate will make our EBCI system reliable to be publicly used.
2. **Robustness and adaptability:** the system should be robust against real-world issues, such as noise and artifacts (e.g., ocular and muscle artifacts) accompanied with EEG recordings. In other words, the preprocessing techniques should be well designed to maintain the accuracy close to its maximum value with very small variations. Furthermore, the EEG is a nonstationary signal depending on the subject state and their emotional and recording conditions. These brain activities signals are less consistent and include many artifacts compared to brain imaging techniques such as CT scans or MRI. Any proposed method for automatic EEG analysis should be able to take into consideration these artifacts to outperform EEG recording classification.

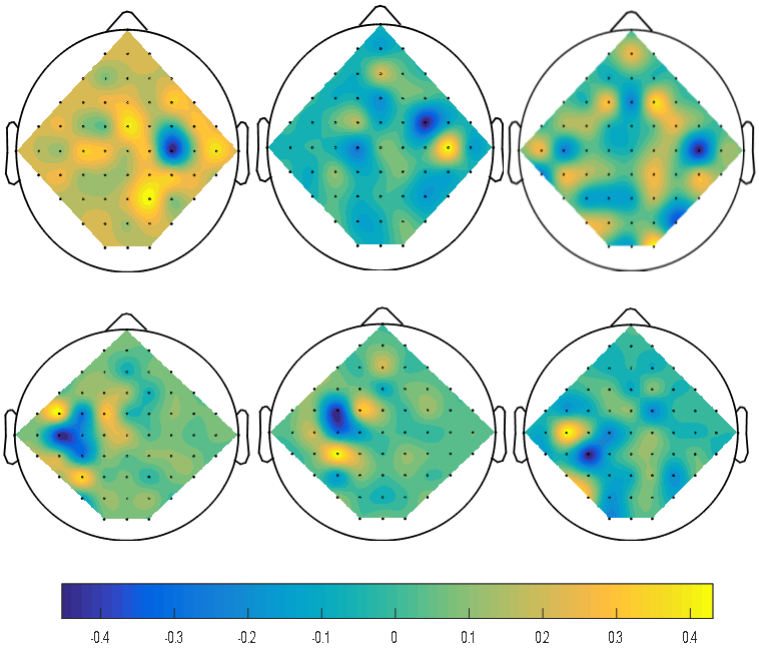

Fig. 8: Specific-subject frequency selection based on ERD/ERS analysis

3. **Power consumption:** one of the main advantages of considering proposed embedded system is to reduce the power consumption of both the prototyping FPGA board as well as its associated acquisition board.
4. **Cost-effective system:** the EEG-based control system should be cost-effective in order to be accepted by a large neurological and scientific community.
5. **Time response:** even if the classification of motor imagery tasks does not have a strict real-time constraint, its time response should be minimized as much as possible. This gives the EBCI system user more flexibility.

4.2. Proposed methodology

In general, the main challenges associated with embedded system design are to satisfy system specifications in terms of limited time response, low cost and complexity, minimum power consumption and other performances such as large bandwidth and high accuracy. Three alternatives can be explored, according to the requirements of the application, as depicted in Fig. 9 [51]. These three alternatives can be summarized as:

- *Embedded software solution:* in this design flow, the application is defined as a software code embedded within FPGA-based hardware architecture, running on the integrated core processors. This solution requires a design of the embedded hardware system with a complete software development environment. If the adequacy of the target architecture and embedded software is sufficient to satisfy the system requirements with respect to the application, this solution becomes very interesting because it allows a rapid virtual prototyping of our application to be completed within a reasonable time and cost. It is assumed that in this case, the timing should not be critical.

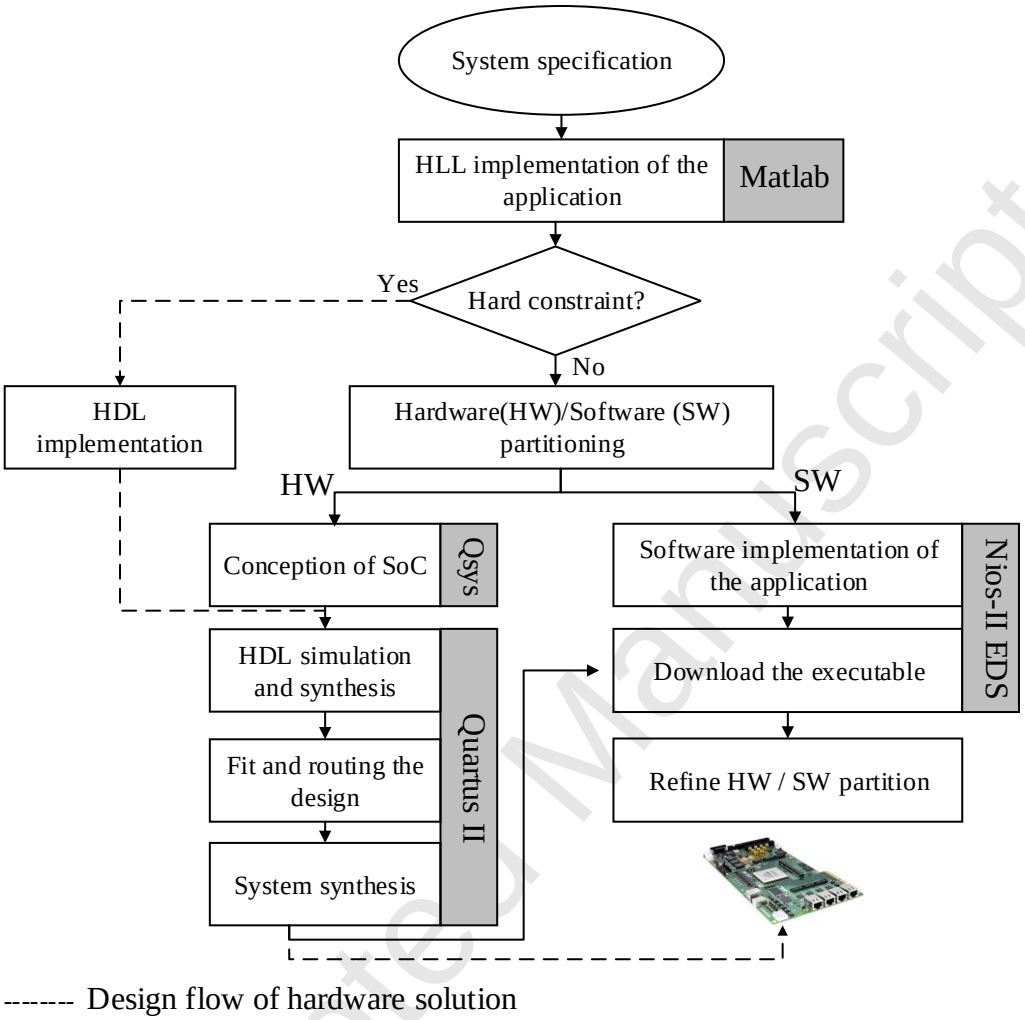

Fig. 9: Design flow of an embedded implementation of BCI system

- *Co-design solution:* this consists of combining both hardware and software components with respect to the embedded system and operating a co-simulation around the FPGA-based processor architecture to meet the timing constraints, which cannot be satisfied by the first solution. In this case, many solutions can be applied using glue logic components, a custom logic instruction approach, and accelerator components for critical functions. The delay will be improved and the complexity of the design is increased. An EEG-based motor imagery is a typical design example which uses such a solution.

- *Pure hardware solution:* this solution is called intellectual property (IP)-based architecture, which is developed using VHDL or Verilog language at the register transfer level to get the complete EEG-based signal processing. This approach can be used when the timing constraints are very stringent and all previous solutions do not meet these requirements. In this case, the IP executes all EEG signal processing. The time to obtain the prototype

is highly important, and the cost of the design complexity and the design time is significantly increased in comparison with those of the previous approaches.

Because our application does not have hard timing constraints, the third solution is excluded from the design exploration. Therefore, our embedded system prototype is developed according to three complementary design flow solutions, which are:

- Design a pure software solution for a functional simulation and test of the complete EEG-based signal processing for motor imagery classification using an offline approach applied on an available dataset via the MATLAB environment. This step is very important to define and to check the global performance of all EEG signal processing chains.

- Export our design into an FPGA-based architecture using the embedded software approach. This solution consists of the design of both the internal hardware architecture based on the fast version of the Nios-II core processor as well as the embedded software code developed using ANSI-C.

- Export the critical parts of the architecture, which are the filters, into a co-processor developed in HDL (hardware description language) while the rest of the architecture, including the calculation of the feature vectors as well as the classification, is implemented in ANSI-C using the GSL library. The entire architectures are co-simulated using the Quartus-II and Nios-EDS environments.

4.3. Design of the EBCI system

The design and implementation of an EBCI system in the context of the SOPC architecture requires the consideration of several issues with respect to the following design flow [51]:

- *Hardware design step:* in this step, the embedded system-based hardware architecture is defined. Altera provides three versions of core processors: Nios-II/s standard implementing a smaller processor with a limited performance, a Nios-II/e economic version designed to use the fewest FPGA logic memory resources and the Nios-II/f fast version with high performance over 300 MIPS. The proposed system incorporates the fast version of Nios-II soft-core processor connected with the other devices through the standard bus interface provided by Altera. This interface is exclusively used to build all Altera system designs to simplify the interconnection and to manage the communication within a complex architecture including a multiprocessor organization.

- *Software design step:* this step consists of the design of an embedded software. The EBCI soft-core application is developed using the ANSI-C language via the Altera Nios-EDS environment. The code is integrated in the FPGA to be executed by the Nios-II processor within the FPGA. Because the proposed system is designed to work in real time, it is important to have a powerful software real-time package to accelerate the execution time of the embedded software. Therefore, the developed ANSI-C code is combined with the GNU scientific library

(GSL) within our embedded architecture. Furthermore, GSL is an open and free C library providing a wide range of mathematical routines that help us to encode complex operators, such as FFT and IFFT of WOLA covariance, eigenvalue, generalized eigenvector, and inverse matrix. The GSL library is compiled using the NiosII-gcc compiler and integrated into the Nios-EDS environment to be run on the host system.

- *System integration step:* both the FPGA-based hardware architecture and the software code have been integrated within the same platform. The code runs on the Nios-II processor within the FPGA. The windowing step of the WOLA method is exported as hardware IP modules to improve the system performance and accelerate the execution time of the proposed system based on the WOLA filter.

The target architecture is based on the FPGA technology built using Altera-tools such as: Qsys for the hardware design components and Nios-EDS (modified Eclipse tools) for the embedded software development. Figure 10 shows the organization of the proposed embedded system, which includes two main layers.

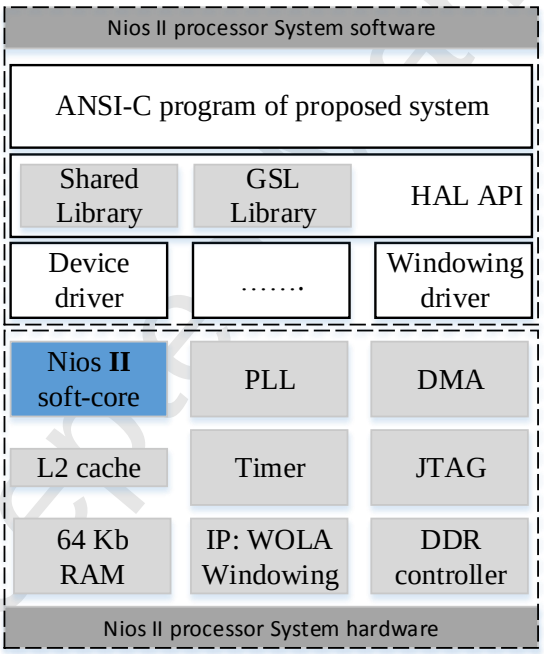

Fig. 10: The proposed embedded system platform

The first layer is the hardware layer depicted in Fig. 11, which integrates the following components:

- The fastest version of the Nios-II, data cache with a size of 64 KB and a 4 KB instruction cache.
- A timer to measure the execution time, with a 32-bit counter, and the time-out period is 10 μs.
- JTAG UART to establish communication between Eclipse and the Stratix-IV board.

- DDR2 memory with 1 GB size, connected to the system design through a DDR2 controller.
- Direct memory access (DMA) to transfer data efficiently, reading and writing data in the maximum space allocated by the source or destination.
- On-chip memory with a size of 4 KB to synchronize data transfer between source and destination through the DMA interface.
- WOLA windowing IP.
- GPIO (UART) to establish the communication between the FPGA and the acquisition system (OpenBCI) to validate the EBCI system according to the online approach.

. In fact, the Stratix-IV development board provides a wide range of advanced memory interfaces such as flash memory with a size of 64 MB, 2 MB of SSRAM, and two DDR2 SO-DIMM sockets supporting a maximum capacity of 8-GB of volatile memory, which are running at 400 MHz. Owing to the large size of EEG data, the EEG signals are stored in the DDR2 memory of the FPGA using a 16-bit format to avoid data distortion, whereas the WOLA coefficients are stored in 64 KB on-chip memory inside the FPGA. These coefficients are used by the windowing IP, for this end that are stored on the internal memory to minimize the time required to access to these data. Furthermore, the EEG signals are sent to the hardware IP via the DMA interface to accelerate the data transfer. The transmission bandwidth of the DMA is approximately 4096×16 bits in a single clock cycle. To window the EEG data by the WOLA analysis block, the Nios-II processor sends an order containing the address of the EEG data to the co-processor, which will recover the signal and weight them with filter coefficients in parallel, as depicted in Fig. 12. An interrupt request is sent to the Nios-II processor, once the EEG data are weighted and stored to a specific address on DDR2, to wake up the processor and apply the remaining routines of the WOLA filter using the GSL library. The effectiveness of the WOLA implementation is verified through MATLAB tools by applying the same data and comparing the two outputs of MATLAB and ANSI-C. In fact, the embedded and high-level language (HLL) implementations give the same results. For the feature extraction and classification algorithms, they are implemented based on the GSL library and they are also validated using a real data [10]. Once the components and their connections are added in Qsys, the HDL files have been generated to implement the instances of each IP in the SOPC. Thereafter, the Quartus-II tool synthesizes the system component to obtain the hardware platform of the proposed architecture.

The second layer of the proposed system is Nios-II processor system software which integrates:

- Device driver of the hardware components such as timer, DMA, and WOLA windowing IP.
- Hardware abstraction layer (HAL) defines software layer allowing a clear distinction between application and device-level software. The HAL API (application program interface) provides services such as file descriptors, I/O control, and buffering, which are required by the ANSI-C library functions.
- All mathematical routines of GSL library are compiled and stored in a single file.

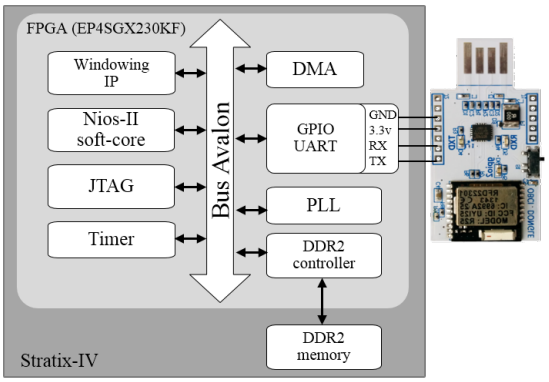

Fig. 11: EBCI-SOPC embedded system

- ANSI-C program contains the main functions of the proposed system, allowing the access to and management of the SOPC components.

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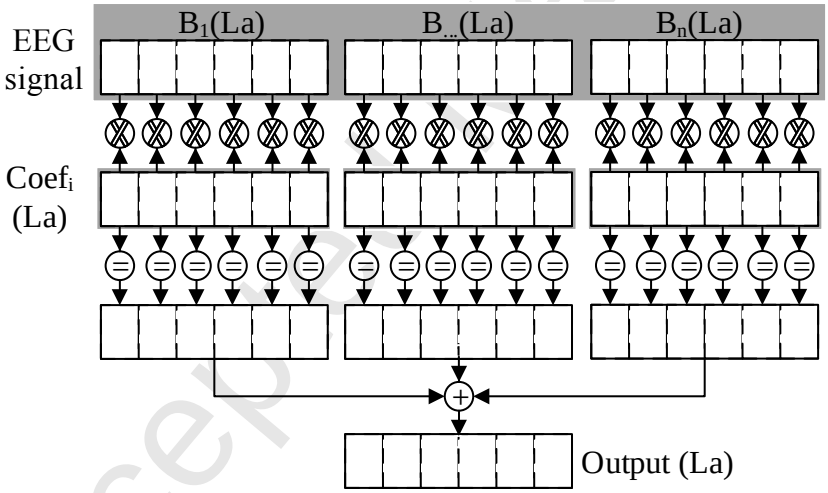

Fig. 12: Internal architecture of the windowing WOLA block

4.4. Evaluation and validation of EBCI system

4.4.1. Offline validation

According to the proposed methodology, the proposed EBCI system is simulated and validated first using the HLL language. In fact, the simulation is performed under the MATLAB environment, using three existing and publicly available datasets from BCI-competition [52, 53, 54]. These datasets are provided by Graz University of Technology. They contain motor imagery EEG signals recorded from seventeen subjects performing two different motor imagery tasks related to left- and right-hand movement. These datasets are organized as follows:

1. Dataset IIa [53], from BCI-competition IV: it consists of EEG data acquired from nine subjects performing four different motor imagery tasks, i.e., LH, RH, foot, and tongue. The data have been recorded in two different sessions using 25 electrodes where three of them contain EOG artifacts. EEG signals were sampled with 250 Hz and filtered between 0.5 and 100 Hz. The recorded data for each subject contain 288 trials. During this study, we have only used EEG signals corresponding to left-hand and right-hand motor imagery (MI) tasks.
2. Dataset IVa [54], from BCI-competition III: this dataset contains EEG signals from five subjects integrating four different motor imagery data i.e., LH, RH, foot and tongue. The data have been acquired through 60 electrodes sampled with 250 Hz and filtered between 1 and 50 Hz. The recorded data contain 80 trials for each class. For our experiment, only EEG signals corresponding to LH and RH were used.
3. Dataset IIIa [54], from BCI-competition III: this dataset contains EEG signals from three subjects integrating three different motor imagery data i.e., LH, RH, and foot. The data have been acquired through 118 electrodes sampled with 1000 Hz and filtered between 0.05 and 200 Hz. The recorded data contain 280 trials. For our experiment, only EEG signals corresponding to LH and RH were used.

4.4.2. Online validation

The implementation of the end-to-end EBCI system requires the interconnection of the EEG signal processing board with a suitable acquisition system. There are several acquisition systems that are more or less complex and whose costs vary significantly. For example, g.Hamp is a high-performance acquisition system, but it is overly expensive and its interfacing requires the development of an appropriate communication interface with our FPGA-based embedded system. The OpenBCI card is another acquisition system, which is cheap and whose specifications seem to be attractive. In addition, interfacing with our FPGA card seems easy enough to set up. The EEG recording is managed by the OpenBCI system, including eight channels with a sampling rate of 256 Hz, where the EEG electrodes have been placed in the scalp according to 10-20 system localization, as depicted in Fig. 13. Four persons participating in these experiments and then are asked to imagine moving their left and right hands by following the MATLAB interface instruction proposed in [55]. The participants are informed by the recording scenario to avoid the risk of suffering owing to the long period of recording [56], which can exceed 30 min. In total, 260 trials are recorded during these experiments, where 140 trials are used for the EBCI training and others to test the proposed system.

5. Results

Once the EBCI system is designed and developed in compliance with the predefined requirements, the next step would be to carry out an evaluation of the system to ensure its effectiveness according to the online and offline approach.

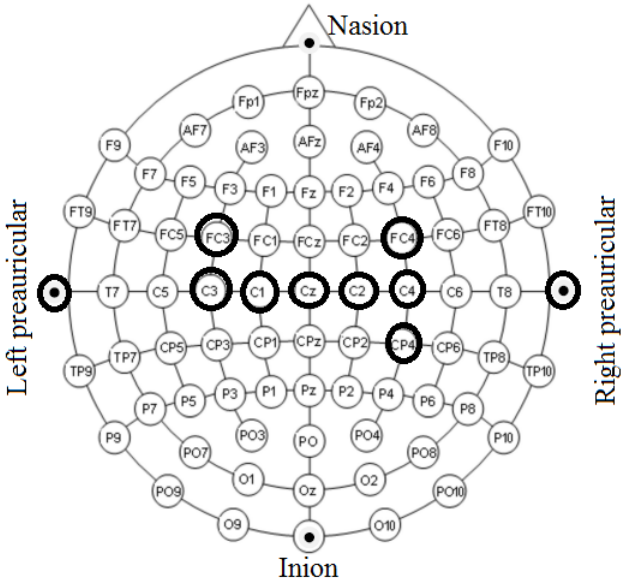

Fig. 13: Locations of electrodes according to the 10-20 system

5.1. Hardware results of the EBCI system

The SOPC containing the required components depicted in Fig. 11 is designed and synthesized using Quartus-II tool of Altera. The hardware resources of the overall system in terms of logic utilization, registers, DSP, and memory block are summarized in Table 3. In fact, the hardware layer of the proposed EBCI system occupied less than 6% of the available resources in the FPGA, allowing the integration of other modules that can accelerate the processing time and allowing the integration of other applications related to BCI in the same chip. In other words, it is possible to migrate the proposed SOPC to other FPGA boards with fewer resources and lower cost. The number of the occupied resources are reduced dramatically compared to the design in [19]. The proposed system design performs with a clock rate of 150 MHz, where the estimated power consumption is close to 0.7 W, as measured by the integrated tool-power analysis of Quartus-II. The power consumption of the EBCI system is also too low compared to the platform proposed in [19].

Resources	Used	Total	Percentage (%)
ALUTs	12025	182400	7
Registers	16556	-	-
Pins	156	888	18
Memory block	820846	14625792	6
DSP	8	1288	<1

Table 3: FPGA resource utilization of the proposed EBCI system

5.2. Software results of the EBCI system

The SOPC is downloaded to the Startix-IV board and connected to the Nios-EDS tools via the JATG interface, allowing the display of the accuracy and the execution time of each block of the proposed EBCI system. Figure 13 shows the execution time of the WOLA filter, feature extraction, and classification algorithm recovered from the Nios-II processor, which operates at 150 MHz. The EBCI system performs a real-time classification of one trial with dimension (500×22) within 430 ms. Furthermore, to extract the specific-subject frequency based on the WOLA method, the system spent approximately 4.6 ms, which represents 1% of the overall processing time. The proposed EBCI system based on the WOLA method is compared to another similar system based on an adaptive filter, which optimizes the filter parameters for each subject to resolve the inter-subject variability problem [19]. The filtering block of the proposed method required 4.3 ms, whereas the adaptive filter spanned 8 ms. In spite of the fact that the delay is short in both cases, in this study, the short time is obtained with minimum resources and consumption. Furthermore, other works mentioned that the time required to filter one trial based on least mean squares and RLS is close to 8 ms and 24 milliseconds, respectively [57]. Otherwise, for comparison purposes and to show the benefits of the proposed methodology based on the hardware/software (HW/SW) approach, the system presented in [58] requires 2 s to perform a trial classification. Another embedded implementation presented in [59] requires 5.2 s to extract and classify the EEG trial captured through only three electrodes.

5.3. System performance of the EBCI system

The overall results of the different specific-subject frequencies selection (SSFS) algorithms are listed in Table 4, showing the system accuracy for each subject according to the offline and the online approaches. As shown in Table 4, the system accuracy is highly sensitive to the SSFS algorithm, where the ERD/ERS analysis method is the most appropriate compared to the other two algorithms. Furthermore, the WOLA method based on ERD/ERS analysis succeeds to maximize the system accuracy, and gives averages equal to 78.85%, 84.28%, 67.28%, and 80.25% respectively, for datasets IIa, IIIa, IVa, and our own dataset. The average accuracy of the proposed EBCI system according to the offline approach is approximately 77%, where for the online approach is 80.25%. Moreover, the results show a good system performance, which reflects the excellent performance of the proposed algorithm and the proposed embedded implementation.

In this paper, we have proposed a practical design exploration for a new application related to real-time, high accuracy BCI system. An embedded architecture, that combines the hardware and software components in a single platform, is proposed to meet the four predefined specifications presented in Section 4.1, which are: high classification accuracy, low power consumption, cost-effective system, and reasonable time response, where the last specification is resolved by integrating a dynamic EEG-filter based on the WOLA technique combined with ERD/ERS analysis methods.

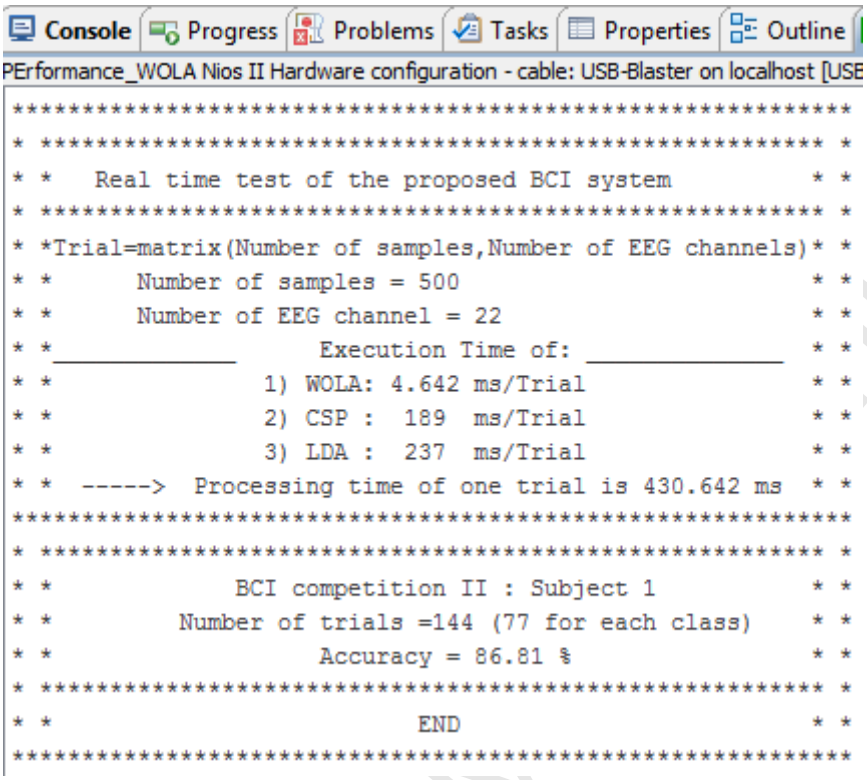

Fig. 14: EBCI system performance for subject *S* 1 of Dataset IIa

5.4. Discussions

The proposed system based on the WOLA and CSP performs autonomous selection of frequency-discriminative EEG characteristics. It is a type of filter bank. For comparison purposes, the performance of the proposed method is compared to the filter bank common spatial pattern (FBCSP) [60]. The architecture of the FBCSP is presented in Fig. 15. The FBCSP algorithm starts by filtering the EEG signal using the Chebyshev filter bank that decomposes the EEG signal into many bands. The second stage performs spatial filtering by linearly transforming EEG signal in each band using the CSP. The third stage performs feature selection of the extracted features using the mutual information best individual features (MIBIF) algorithm. In our case, the selection of the best individual information is performed during the filtering process instead of using it during the feature extraction steps. For this reason, the proposed method has a low complexity and short processing time compared to the FBCSP, as depicted in Table 5. The complexity of the two architecture is measured using the *profile* statement of MATLAB, which is executed on laptop running at 2.7 GHz. The estimated time is measured for one trial with a dimension of (500×22), where 22 is the number of channels.

The test set performance of the FBCSP and WOLA-CSP algorithms on the evaluation data (second session of

SSFS	S1	S2	S3	S4	S5	S6	S7	S8	S9
Offline approach: Dataset IIa									
HT	72.08	54.52	82.33	62.08	65.55	64.91	66.63	94.58	88.86
SNEO	67.91	54.91	84.83	65.69	58.08	68.75	74.94	92.63	88.86
ERDSA	86.81	63.89	94.44	68.75	56.25	69.44	78.47	97.91	93.75
Offline approach: Dataset IIIa									
HT	86.11	55	76.66						
SNEO	89.44	60.33	78.33						
ERDSA	97.77	61.66	93.33						
Offline approach: Dataset IVa									
HT	64.39	94.64	50	69.64	49.64				
SNEO	65.32	95.71	49.29	71.07	50.71				
ERDSA	66.79	96.07	52.14	71.43	50				
Online approach									
GD	69.3	71.66	78.33	82.5					
SNEO	70.83	74.16	82.5	76.66					
ERDSA	72	75	85	89					

Table 4: System accuracy for different specific-subject selection algorithms for each subject

Techniques	Frequency step (Hz)	Number of instruction	Estimated consuming time/trial (s)
WOLA-CSP	1	1827	0.165
FBCSP	4	6164	0.852
	2	12328	1.7
	1	24656	3.4

Table 5: Complexity estimation of FBCSP and WOLA-CSP

each dataset) in terms of accuracy values is shown in Table 6. Three configurations of filter bank are used, where the first decomposes the EEG into many multiple pass-bands with a step of 1 Hz, the second with step of 2 Hz, and the third with a step of 4 Hz. The results show that apart from subject 5 of dataset IIa, the proposed method outperformed the FBCSP with a step of 1 Hz, often substantially. For dataset IIa, the proposed method outperformed FBCSP with the step of 1 Hz by approximately 8% in mean classification accuracy. For datasets IIIa and IVa, the WOLA method based on CSP outperformed by approximately 10% and 3%, respectively. Hence, the WOLA technique resolves the nonstationarity problem and the inter-variability between subject, while consuming fewer computing resources and

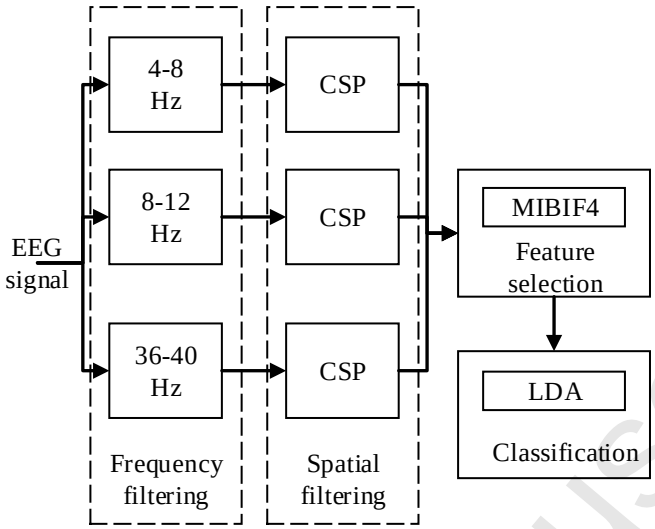

Fig. 15: Architecture of the FBCSP algorithm for two-class motor imagery EEG data

less power.

Frequency step (Hz)		S1	S2	S3	S4	S5	S6	S7	S8	S9
Dataset IIa										
WOLA-CSP	1	86.81	63.89	94.44	68.75	56.25	69.44	78.47	97.91	93.75
FBCSP	1	82.63	51.38	85.41	54.16	60.41	56.25	67.36	89.58	88.19
	2	79.16	60.41	93.05	56.94	75.69	61.11	76.38	90.27	88.88
	4	87.50	57.63	88.88	61.80	77.08	61.11	85.41	92.36	86.11
Dataset IIIa										
WOLA-CSP	1	97.77	61.66	93.33						
FBCSP	1	97.77	55.55	91.11						
	2	96.66	61.11	94.44						
	4	93.33	53.33	93.33						
Dataset IVa										
WOLA-CSP	1	66.79	96.07	52.14	71.43	50				
FBCSP	1	53.6	85.8	50	49.10	48.40				
	2	71.4	100	60.7	49.10	48.40				
	4	68.7	100	59.2	49.10	48.40				

Table 6: Accuracy obtained by the WOLA-CSP and FBCSP for different frequency step

6. Conclusion

This paper proposes an efficient HW/SW implementation for an EBCI system based on motor imagery, including training and testing steps. The proposed system employs the filter bank techniques based on WOLA and CSP as a feature extraction algorithm and LDA as a classifier. The WOLA method is used to dynamically filter the EEG signal by taking the most active components containing the ERD/ERS events related to left- and right-hand movements. This method considers the state of the subject by analyzing the ERD/ERS component before and during the left- and right-hand movements. Our results show a clear improvement in the system performance by integrating the WOLA method into the EEG chain. Another advantage of the WOLA technique is its lowest processing time compared to other existing filter techniques, such as FIR, IIR, and RLS. The processing time of one trial by the proposed EBCI system is approximately 0.4 s, which is too fast compared to other EBCI systems. Due to the significant improvement of the classification accuracy, processing speed, embedded implementation, and low development cost, this programmable hardware embodies a good BCI platform and opens new research opportunities and interests in further useful applications related to the disabled or severely impaired persons. As future work, we will explore other techniques related to cognitive frequencies that can be used to localize the EEG artifacts related to eye blinking, muscle activities, EOG, etc. Furthermore, the proposed HW design could be exported as an ASIC to minimize the size of the system, as well as to decrease its power consumption.

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