An embedded Implementation of home devices control system based on brain computer interface

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***Abstract* – This paper presents a new embedded architecture for home devices control system directed through motor imagery actions captured by EEG headset. The proposed system is validated by an offline approach which consists on using available public data-set. These recording are always accompanied with noise and useless information related to the equipment, eyes blinking and many others resources of artifacts. For this reason, a complex EEG signal processing is required; starting by filtering EEG to keep the frequency of interest which is located on µ-rhytm and β-rhytm bands in our case; followed by the extraction of useful feature to minimize the size of EEG data and enhance the probability of classifying each trial correctly. A prototype of our proposed embedded system has been implemented on Stratix IV FPGA Board. The prototype operates at 200 MHz and performs real-time classification with an execution delay of 0.5 second per trial and an accuracy average of 72%.**

Keywords – brain computer interface (BCI), electroencephalogram (EEG), EEG filters optimization, Motor imagery

I. INTRODUCTION

The aim of Brain Computer Interface (BCI) is to completely build a new communication pathway between brain and electronic devices to restore capabilities for people with severe motor disabilities. Fig 1 depicts an overview of our proposed system which helps a handicap person to control home devices. User must provide different brain pattern activities which will be captured through a non-invasive EEG headset based on Ag/Cl sensor. The captured data is then processed using an electronic system to translate each thinking actions to actuators for home devices control purpose.

The proposed home devices must be embedded into systems to meet stringent requirements directed by BCI application [1]. The system should perform real time signal processing to extract critical information early in the data stream and minimize as possible the system latency [2]. Also, the system should be miniaturized to enable the subject to interact freely with the surrounding without any risk of discomfort. Furthermore, home devices applications should consume low power and should be reconfigurable, portable and flexible. For all these reasons, a general purpose processing platform is inconvenient to meet these constraints [3] and so it is necessary to look for a suitable architecture to achieve efficient processing and practical applications.

Nowadays, several BCI researchers continue to find and to improve solutions for practical implementation of BCI processing algorithm. In the literature, many BCI applications are implemented using advanced platform as DSP, ARM and FPGA. There are some studies which focus on the implementation of only one block from the basic BCI chain.

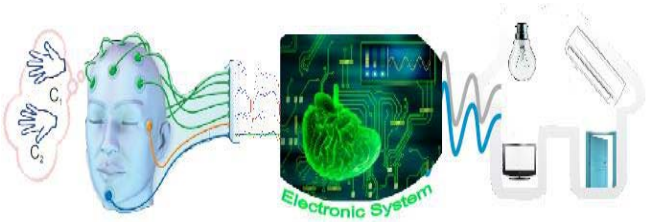

Figure 1: Proposed home devices system

For example, a spatial algorithm known as ICA (Independent Component analysis) is implemented on an FPGA to accelerate its execution time which is very slow when it's running on general-purpose processing platform [4]. Others researchers implement an adaptive filter to process EEG signals in real time and remove artifacts [5]. On the other hand, there are some studies which implement a full BCI chain from filtering EEG data to the classification of different trials [1, 6, 18]. Most of the published works are focusing on the Steady-state Visual Evoked Potential SSVEP, which is an EEG signal response to the flickering visual stimulus. This technique is used to control hospital bed nursing system [6]. The system firstly presents a light emitting diode stimulation panel to induce the user's SSVEP signal which will be processed in FPGA and translated to corresponding actions. Similarly, home devices systems are developed based on the SSVEP approach using computer-based architecture [7] and ARM processor [8]. Despite the successfully implementation of mentioned homes devices system, the obtained product is discomfort and prevent the uses of the system freely.

In this paper, we propose to implement a new home device system based on FPGA architecture to control basic home devices by the thought of two motor imagery actions. User must provide two activities: think move Left Hand (LH) and Right Hand (RH) correspond to class one and two respectively. The main objective of the electronic system is to extract the thinking actions to be translated to electric command of door, light…etc. The proposed system is

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validated on the public data set of BCI competition III. The proposed motor imagery approach, using home device based-on FPGA embedded system will be more comfortable and allows subjects to use it freely.

The remainder of this paper is organized as follows. In Section 2, fundamentals of BCI theory is described. The SoC FPGA-based design architecture for the proposed home device system is explained in section 3. Section 4 presents the simulation and realization of the system. The conclusion and future works plans are discussed in Section 5.

II. Overall Brain Computer Interface Description

The general structure of the brain computer interface system is depicted on Figure 2. As a first validation of the proposed system, we consider the offline approach which consists of using existing EEG data-sets. In all our experiments, we use the data set (IIIa) of BCI Competition III [9]. These data were provided by Graz University of Technology and were recorded from nine subjects performing four different motor imagery data, i.e., LH, RH, foot and tongue. The recording was done with 25-channels. Three of them contain EOG artifacts. The EEG was sampled with 250 Hz, and filtered between 0.5 and 100 Hz. Each subject recording contains 288 trials. For this study, we use only EEG signals corresponding to LH and RH tasks. First, trials are extracted in reference to the Trigger during 2 seconds based on some experiments. For each subject EEG data are divided into two parts: training part and test part; which are stored into memory file and loaded into FPGA later. Then, we proceed by filtering blocks which is a useful preprocessing step for removing artifacts and improving stationary. The unwanted signals should be removed carefully using one of the appropriate filtering techniques [19]. The most effective and widely used algorithms of EEG data filtering are Finite Impulse Response (FIR) and Infinite Impulse Response (IIR). In our case we use FIR filter which is simpler and more convenient for programming on dedicated digital signal processing platform.

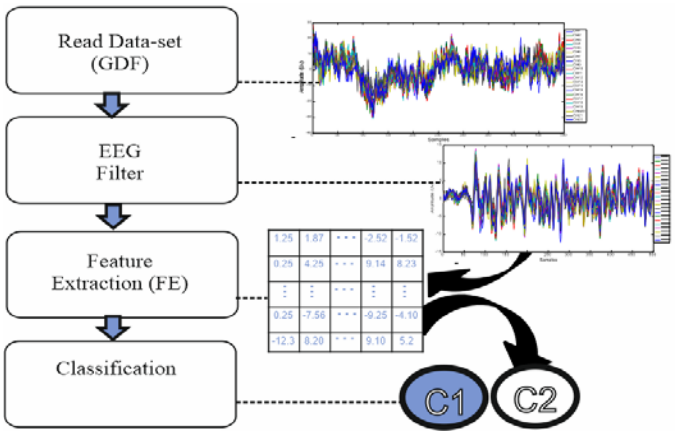

Figure 2: System block diagram of EEG chain

We use Butterworth filter with order 4 to remove the data outside the theoretical frequency response located on the μ-rhythm [8-13] Hz and β-rhythm [14-30] Hz [10]. In the third step, we proceed for the examination of long recordings of EEG signals which requires rapid and automatic methods to provide fundamental features to be used in subsequent automatic analysis. Many techniques have been reported including power spectral density, Short-Time Fourier transform STFT [10], Common Spatial Pattern CSP [11] and wavelet analysis [12] etc. The choice of any technique will affect the accuracy of the associated classifier. In this respect, we will consider the CSP technique which is the best spatial filter algorithm for motor imagery from the effectiveness point of view to extract ERD/ERS effects. The main idea of this technique is to design a pair of spatial filters such that the filtered signal's variance will be maximal for one class while minimum for others. The returned algorithm is known by its highest computation complexity and isn't yet embedded. It is a major issue of embedded-real-time implementation of CSP in the BCI domain.

Finally, the classification block is provided to classify each trial to its corresponding actions. A comprehensive review of classifiers for BCI is presented in [13] with many classifiers algorithm such as Linear Discriminant Analysis (LDA), Support Vector Machine (SVM), Neural Networks (NN), Hidden Markov Models (HMM) and Mahalanobis distance (MD). The MD technique, which is a variant of the LDA techniques, is addressed by our experiments and for which we have assigned a feature vector x for the class that corresponds to the nearest prototype. It is a simple and robust classifier and seems to be suitable for asynchronous BCI systems. Despite its good performances, it is still scarcely used in the BCI literature. The returned MD algorithm is too fast compared with other algorithm such as SVM, LDA, HMM and KNN.

The first validation step of the proposed system consists on developing and simulating Matlab codes. Figure 4 presents the performance of the system which determined by the mean of the classification accuracy, sensitivity and specificity over 5 runs for the nine subjects. The proposed approach outperforms significantly performances reported in the literature [14].

III. Embedded Implementation of Home Device System

The design and implementation of a real-time home devices control system in the context of SoC (System on Chip) architecture require consideration of several issues such as: hardware design step, software design step and system design step [15]. In the first one, the embedded system-based hardware architecture build around embedded soft-core processor as depicted on figure 3. It incorporates fast version of the Nios II core processor with on-chip memories and a JTAG-UART interface interconnected using the Avalon fabric. We use DDR2 memory because it is the only memory on the board that can support the calculation of the matrix with biggest size. Then, we proceed for the design of a pure software architecture using Gnu Scientific Library (GSL) based-on high-level language (HLL). We chose an existing

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ANSI-C library due to the hard complexity of BCI algorithm, especially CSP. The code is developed and executed first on Intel processor platform. Once simulated and checked, we integrate all BCI codes on the Nios II processor to be executed. Finally, we integrated our design in FPGA-based architecture including both hardware and software components. The Altera Stratix IV EP4SGX230KF40C2 technology is used here for the prototyping. To accelerate the execution of our proposed system, an adequacy between the architecture and target techniques is explored by performing several optimizations: On the system architecture, we maximize the cache memory size and use burst option to send the data from memory to processor. On the software level, we minimize the number of instructions and inter-space the interdependent operations.

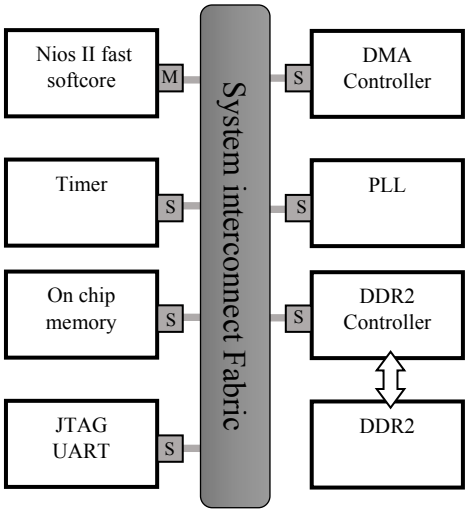

Figure 3: Block diagram of the home device SoC

IV. Experimental Implementation and Validation

After integrating the overall architecture including hardware and software in a single Chip, we have simulated the design and evaluated their complexity. Table 1 presents the complexity of a total system with their hardware and software parts in term of Logic utilization (LUTs), DSP and block memory. We note that the complexity of the design is too low compared to available resource. The whole home devices design occupied less than 7% allowing the possibility of integrating hardware IP to accelerate EEG signal processing and to integrate other BCI techniques.

FPGA core resources type	Resources of EP4SGX230KF40		
	Used	Total	Percentage
LUTs	17281	456000	7%
Block memory	557.332	14.625.792	4%
DSP block	4	1288	<1%

Table 1: Resource utilization of the Startix IV FPGA

For validation purposes of our proposed system, we use Matlab 2010a to check the accuracy of classification regardless the timing consideration for different trials. Using Matlab, the system performance reach about 80% for nine subjects as depicted on Figure 4. In order to test the system with full speed operation (200 MHz), EEG data were uploaded to the DDR2 of Stratix IV FPGA using double formatted data to avoid any information loss. We notify that, extracted data features from the FPGA-based architecture are exactly the same as the resources extracted using the Matlab simulation. Once downloading the hardware design on the board, ANSI-C code of home devices are launched on the Nios II processor which is connected to Eclipse Window through JTAG interface to show the results of classifier. As depicted in Figure 4, performances of the control home devices system based on FPGA are very reasonable compared with Matlab. Indeed, the average accuracy of classification for the nine subjects is about 72%. This small difference in the accuracy is due to diverse factors at feature extraction and classification levels. We use the CSP at the feature extraction level which is based on generalized Eigen vector problems. This type of operation is too complex, and it is not easy to find the same results as Matlab. In addition, the classifier uses the calculation of the inverse of the square matrix, which is also a complex operation when using a big size matrix, or if the matrix is badly scaled. We notify, that Matlab environment is too accurate with respect to GSL Library. Despite this complexity of the proposed architecture, the proposed home devices system processed EEG data in real time and provides good performance.

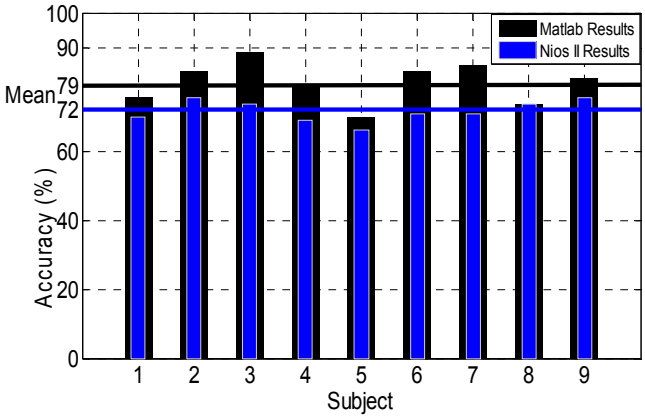

Figure 4: Accuracy of the home devices system

The timing presenting in Fig5 is provided by the Nios II soft-core CPU, the measurements are taken through highly accurate internal timer. As depicted on the Figure 5, the proposed home devices system takes about 57.77 seconds during the training process based on 106 trials. These results mean that to classify an action, the system will take about 0.5 second to process one trial. Despite that for home device applications, we don't have strong real-time constraints, the processing time of our system on chip is smaller than the execution time for several embedded systems in same applications domain. For example, to control hospital Bed nursing system based on SSVEP approach, the system proposed in [6] takes about 5.2 seconds to process one trial

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while it based-on a very simple algorithm and uses only 3 channels (in our case we use 22 channels). Furthermore, others work mentioned the timing spanning to process one EEG trial captured based-on 5 channels is about 3 seconds [16].

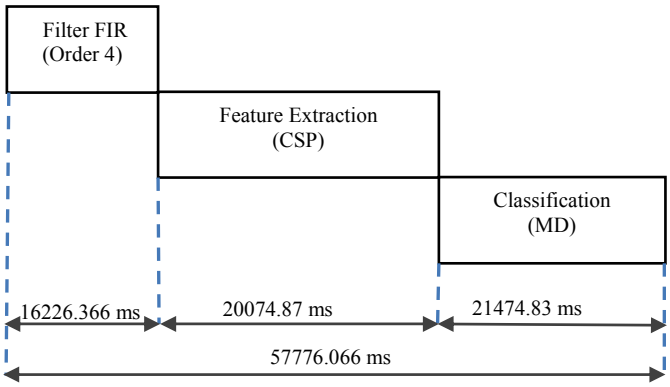

Figure 5: Execution time of training home devices system

V. Conclusion

In this paper, we present an issue of a first hardware software implementation of entire brain computer interface chain including training and classification steps. We demonstrate the feasibility of an embedded home devices system based-on FPGA and commanded through the thought of two motor imagery actions. The proposed methods achieve an acceptable system performance with an execution delay of 0.5 second per trial with very low FPGA resources. In future works, we will add additional filters to enhance the SNR of the processed data which will increase the system performance. The development of a full integrated architecture including hardware accelerators to enhance the execution time is in progress.

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