SmartEEG : a multimodal tool for EEG signals

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***Abstract*—In this paper we present an hardware realisation for an image coder used in the SmartEEG project. This collaborative project has the aim of the conception of a multimodal tool for EEG signal to allow transmission of a complete examination of a patient. We show that we can expect good performance on a FPGA board for the time consuming part of this tool that is the image coder.**

I. EEG

A. Neurophysiology

Situation of functional explorations in neurophysiology deteriorates in a preoccupating way. On one hand, the number of examinations increase, in particular because of the ageing of the population, which leads to an increase of the number of people affected by neurological disease. On the other hand, the number of neurophysiologists are decreasing. Therefore neurophysiologists are missing, in a temporary or permanent way, in hospital and the potential of neurophysiological examinations is clearly a matter of preoccupation.

This situation is even worse in emergency services, intensive care services and about organ donations.

Nevertheless World Health Organisation has identified neurophysiology as one of the fundamental discipline of medical specialization considering the numerous invalidating and grave pathologies where it intervenes. Only the electroencephalogram (EEG) allows the diagnosis and the appreciation of the severity of a number of pathologies:

- Epilepsy, state of epileptic.
- Diagnosis of a state of brain death.
- Disorders of the consciousness and the vigilance.
- Sleeping disorders.
- Encephalitis necrotizing as the meningoencephalitis herpetic, metabolic or toxic encephalopathies.
- Creutzfeldt Jakob disease.
- Premature children follow-up.
- Brain damage echo (Brain haemorrhages, ...).

As underlined by the WHO, EEG is a complementary modality of imaging methods which has very important perspectives. It is portable, less intrusive because does not emit radiations, it allows to realize examinations with a low cost equipment.

It is an ideal tool, in particular for mobility situations in industrialized countries, as well as for the developing countries of South-East Asia and Africa. Especially, it does not return the same services, because contrary to the brain imaging, it is capable of highlighting intellectual dysfunctions - even without visible lesion - which remain the only anomalies met in certain pathologies.

B. Stake

In France, 500 000 patients suffer from epilepsy for an annual estimated cost of 3,5 billion euros including approximately 500 000 consultations. Furthermore, 90 % of transplantation are realized following a donation of organ resulting from a subject in encephalic death validated by two EEGs with flat record at 4 hours apart.

There is thus today a stake in health service to ensure the interpretation of the neurophysiological exams in delays compatibles with the medical requirements taking into account human resources.

Like other medical specialities, remote interpretation brings an answer in this stake. For that purpose, it is necessary that the neuropsychologist who makes a remote expertise have a complete recording of the examination which was made. This recording must include an EEG plot, an ECG plot, comments of the pratictionner or the technician who has proceeded to the examination, and an audio and video recording of the examination which is essential to know the flow of the examination.

Video helps in making the link between the setting of abnormal movements of the patient and the modification of the EEG signal. It then allows diagnosis of artefacts. Other types of information as the therapeutic history or the measure of physiological signals are also

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necessary to make the diagnose. Finally the measure of the observance is an important additionnal information.

II. SmartEEG

Aim of the SmartEEG project is to realize a tool to monitor multimodal ExG signals, audio and video, and to enable a remote analysis of these signals.

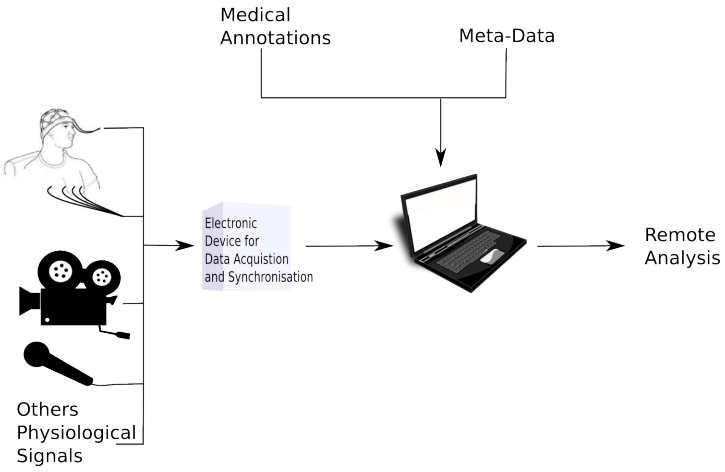

Fig. 1. SmartEEG system

SmartEEG system is depicted in figure 1. One of the main challenges of this realisation is the generation of a synchonized flow of ExG signals (ElectroEncephaloGram, ElectroCardioGram) video, audio and other physiological signals.

This synchronisation is a difficult challenge because we want to monitor patient movements, even the smallest and the quickest, typical timing is 10 ms, and then it is mandatory to use high performance image compression algorithm for video sequence for remote transmission that keep high frequency movements.

Compression algorithm choice is then a point of interest here.

In SmartEEG we use a lossy image compression algorithm based on wavelet transform which have a good perceptual quality, based on SSIM [1] measures.

In the next section we describe this algorithm.

III. Image Compression

A typical image compression scheme visible on figure 2 manipulates the input image data to obtain an uncorrelated representation of the image, on which an entropy coder is applied to reduce bits by identifying and eliminating statistical redundancy. Since the non-stationarities inherent in the image data would affect the effectiveness of coding procedure, several enhanced entropy techniques have been developed such as context based arithmetic coder [2] and its modifications.

Although these coders are efficient and are widely used in the image compression applications such as JPEG2000 [3], by modeling the image as a stationary source, they are suboptimal and yet the performance of these methods deteriorates significantly in non-stationary areas like edges.

To overcome this weakness, enumerative coding was first introduced by T. J. Lynch and L. D. Davisson [4], [5]. This lossless coding method can be used to effectively encode source sequences without requiring explicit source statistics and easily adapt to variations in the statistics. However, it did not become popular in practical compression applications due to the computationally complex nature of baseline procedure, which requires to encode with large block size.

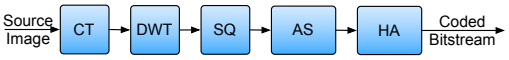

Fig. 2. Algorithm Compression Scheme

To solve the problem Waaves coder from CIRA uses a hierarchical approach to enumeration which provides efficient compression of locally stationary binary signals. In contrast to traditional enumerative coding, this approach does not use any specific statistics. It could encode the side information by repeated use of enumerative coding, thus it may enable the usage of small block size coding and provide robustness against regional variations in image statistics.

Performance of this approach were compared with the results of context-based arithmetic coding as well as the LZW coding, experiments showed that hierarchical approach can obtain 8% less size on the coded stream rather than arithmetic encoder for locally stationary binary source. The possible applications of the method include compressions of the binary image and the overhead information in video and image coding, as well as compact representation of the locations of significant wavelet coefficients in wavelet based compression.

An overview of the image encoder that depicts hierarchical approach is illustrated in figure 2. First, the pixel component transformation is applied to the input image and each input pixel is converted from the RGB color space to the YCbCr color space. Then, each component is individually transformed by a 2-D DWT using a CDF 9/7 wavelet basis and quantized by scale value for the coefficients. Next, each sub-band is fed into the adaptive scanning block and the quantized coefficients are adaptively reorganized into 1-D array for the purpose of maximizing the local stationarity. Finally, the sorted coefficients are encoded by hierarchical approach in the

inner loop bit plane by bit plane.

Prior to hierarchical approach a rearrangement phase is necessary, we call it Adaptive scanning in Waaves coder. Adaptive scanning scheme leverages an efficient exploration of the correlation among inter-band or intra-band wavelet coefficients to increase the compression efficiency.

We compared Waaves coder with two state-of-the-art JPEG2000 coders, Lurawave and ACDSee [6]. In our experiments, both the Peak Signal to Noise Ratio (PSNR) measure and the Structural SIMilarity (SSIM) measure [1] of four images were evaluated using a MSU Video Quality Measurement Tool [7]. Compressed image quality was chosen to get approximately same size of output file for all codecs. Our test results are depicted in Table I. We observe that the Waaves coder has higher PSNR than Lurawave. Although the PSNR of Waaves coder is sometimes lower than ACDSee, they are very close to each other. Regarding the SSIM index, as SSIM index has been developed to have a quality reconstruction metric that also takes into account the similarity of the edges between the denoised image and the ideal one, it has become a widely-used image quality assessment metric which is considered to provide a better quality measurement than the PSNR. The Waaves coder shows overall better results than the two JPEG2000 coders in terms of SSIM.

If we evaluate processing time of Waaves encoder on a Xeon 8-core CPU running at 2.4GHz, it spends more than 500 ms to encode 512x512 RGB image, same test has been done on a TI Integra C6A816x DSP+ARM processor running at 1.5GHz, the processing time is 2 s. Therefore, the acceleration is necessary. If we realize a profiling of the application we can notice that hierarchical approach and Adaptive scanning take more than 70% of the total computing time.

These part of image coding algorithm employ intensive memory access which results in poor performance on the embedded DSP architecture. It is the reason that motivates the use of FPGA-based accelerators where we can have the embedded block memories or off-chip memory fetches through direct memory access (DMA). Such accelerators have been successfully used for applications with large memory access patterns.

In FPGA we can integrate System-on-Chip (SoC) combining with processor and hardwired intellectual properties (IPs) that allows efficient acceleration of compute/memory-intensive tasks and appropriate adaption to an embedded system which requires low power consumption, it also provides the advantage of the feasibility to be fully integrated as ASIC. Our work is the first hardware implementation of hierarchical approach combining parallel processing and data access optimization to avoid communication and idle time during processing.

We describe the FPGA based SoC architecture and present experimental results.

TABLE I
PSNR AND SSIM WITH QUANTIZATION PARAMETER = 10

Image	PSNR (dB)			SSIM		
	Waaves	Lurawave	ACDSee	Waaves	Lurawave	ACDSee
Flower	43.8483	42.1703	43.1402	0.9882	0.9785	0.9825
Sailboat	44.3472	42.8920	44.7435	0.9888	0.9809	0.9866
House	43.9114	42.2677	44.8325	0.9859	0.9785	0.9837
Parrot	44.3102	41.6757	44.9829	0.9810	0.9699	0.9785

IV. WAAVES HARDWARE IMPLEMENTATION

We have realized a system on chip based on codesign plateform shawn in figure 3, and implented it on a Stratix IV FPGA DE4 board from Terasic shown in figure 4.

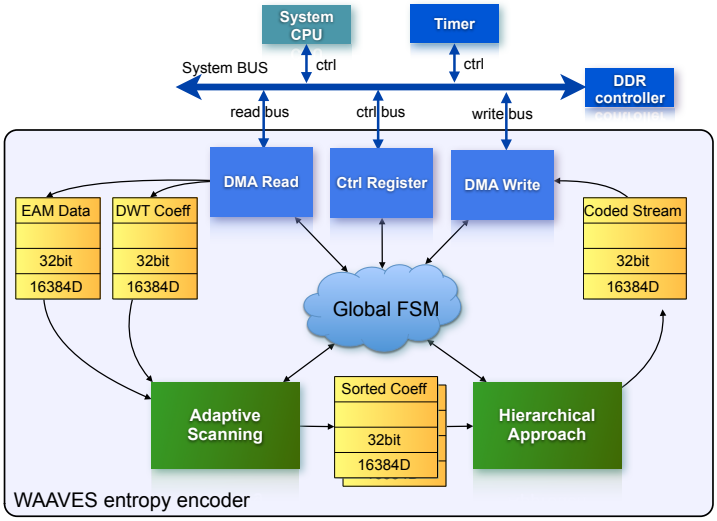

Fig. 3. System on Chip for image compression

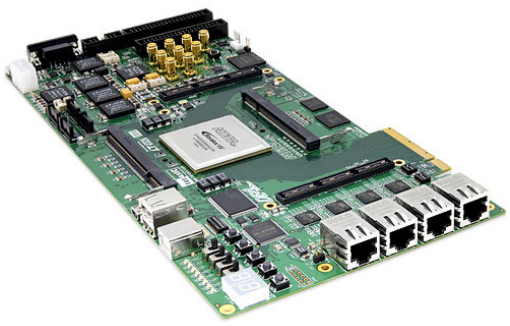

Fig. 4. System on Chip development board

The Adaptive scanning block and hierarchical approach block takes more than 70% of the total time of execution. For this reason we have designed hardware accelerator of these two blocks connected to a system bus by two Direct Memory Access, one for read access and another for write access.

A CPU take in charge the rest of the algorithm.

V. Result

We present here results for the two hardware IPs developped to accelerate our compression algorithm.

In the table II we show result of hierarchical approach. An acceleration of more than 9 if we compare to a recent DSP processor, and more than 5 compared to Xeon single core processor at 2.4 GHz.

TABLE II
HIERARCHICAL APPROACH LATENCY AND SPEEDUP IN DIFFERENT IMPLEMENTATIONS

512×512 grayscale	Xeon CPU @2.4 *GHz*	DSP @1.5 *GHz*	1PU hierarchical approach *@100 MHz*	4PUs hierarchical approach @100 *MHz*
latency	45.57 *ms*	98.7 *ms*	14.3 *ms*	4.6 *ms*
speedup	1	0.46	3.2	9.9

In table III results of Adaptive scanning accelerator are shown. We can notice that for encoding a subband of 128x128 our accelerator obtains same performance than a Xeon single core processor at 2.4 GHz if it is clocked at 100 MHz.

TABLE III
ADAPTIVE SCANNING LATENCY AND SPEEDUP IN DIFFERENT IMPLEMENTATIONS

512×512 grayscale	ARM CortexA9 @666 *MHz*	HW Adaptive scanning @100 *MHz*
latency	133.76 *ms*	10.69 *ms*
speedup	1	12.8

The total processing time on a 512x512 grayscale image on our FPGA based platform takes 48 ms with a clock rate at 100 MHz.

VI. Conclusion

We have presented here an implementation of a high performance image compression algorithm that enables a real-time monitoring of a patient with EEG and ECG We need to accelerate the processing time of the image compression algorithm by using duplication and with higher clock frequency to reach the goal of SmartEEG project that is 10 ms per image. The next step in our work is to synchronize this image flow with ExG signal, audio signal and other physiological signals.

VII. Acknowledgment

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